CLAIMS

What is claimed is:

1. A method comprising:

providing a semiconductor substrate that includes a memory container having a double-sided capacitor; and

vapor phase etching a layer adjacent to the side wall of the memory container with a vapor having a surface tension lowering agent.

2. The method of claim 1, wherein vapor phase etching the layer adjacent to the side wall of the memory container with the vapor having the surface tension lowering agent comprises vapor phase etching the layer adjacent to the side wall of the memory container with the vapor having a carboxylic.

3. The method of claim 1, wherein vapor phase etching the layer adjacent to the side wall of the memory container with the vapor having the surface tension lowering agent comprises vapor phase etching the layer adjacent to the side wall of the memory container with the vapor having a carboxylic.

4. The method of claim 1, wherein vapor phase etching the layer adjacent to the side wall of the memory container with the vapor having the surface tension lowering agent comprises vapor phase etching an oxide layer adjacent to the side wall of the memory container.

5. The method of claim 1, wherein vapor phase etching the layer adjacent to the side wall of the memory container with the vapor having the surface tension

lowering agent comprises vapor phase etching a borophosphosilicate glass (BPSG) material adjacent to the side wall of the memory container.

6. The method of claim 1, wherein vapor phase etching the layer adjacent to the side wall of the memory container with the vapor having the surface tension lowering agent comprises vapor phase etching the layer adjacent to the side wall of the memory container with the vapor having hydrogen fluoride and an etch initiator composition.

7. A method comprising:

providing a semiconductor substrate that includes a double-sided capacitor memory container; and

etching a layer adjacent to a side wall of the double-sided capacitor memory container with a vapor that includes methanol.

8. The method of claim 7, wherein etching the layer adjacent to the side wall of the double-sided capacitor memory container with the vapor that includes methanol comprises etching an insulator layer adjacent to the side wall of the double-sided capacitor memory container with the vapor that includes methanol.

9. The method of claim 7, wherein etching the layer adjacent to the side wall of the double-sided capacitor memory container with the vapor that includes methanol comprises etching a doped oxide layer adjacent to the side wall of the double-sided capacitor memory container with the vapor that includes methanol.

10. The method of claim 7, wherein etching the layer adjacent to the side wall of the double-sided capacitor memory container with the vapor that includes methanol comprises etching an insulator layer adjacent to the side wall of the double-sided capacitor memory container with the vapor that includes hydrogen fluouride.

11. A method of fabricating a semiconductor substrate, the method comprising:

placing a semiconductor substrate that includes a double-sided capacitor container in a chamber; and

vapor phase etching a layer adjacent to a side wall of the double-sided capacitor container with a vapor that includes hydrogen fluouride, an etch initiator composition and an alcohol.

12. The method of claim 11, wherein vapor phase etching the layer adjacent to the side wall of the double-sided capacitor container with the vapor that includes hydrogen fluoride, the etch initiator composition and alcohol comprises vapor phase etching an oxide layer adjacent to the side wall of the double-sided capacitor container with the vapor that includes hydrogen fluoride, the etch initiator composition and alcohol.

13. The method of claim 11, wherein vapor phase etching the layer adjacent to the side wall of the double-sided capacitor container with the vapor that includes hydrogen fluoride, the etch initiator composition and alcohol comprises vapor phase etching an insulator layer adjacent to the side wall of the double-sided capacitor container with the vapor that includes hydrogen fluoride, the etch initiator composition and alcohol.

14. The method of claim 11, wherein vapor phase etching the layer adjacent to the side wall of the double-sided capacitor container with the vapor that includes hydrogen fluoride, the etch initiator composition and alcohol comprises vapor phase etching a layer adjacent to the side wall of the double-sided capacitor container with the vapor that includes hydrogen fluoride, the etch initiator composition and a methanol.

15. The method of claim 11, wherein vapor phase etching the layer adjacent to the side wall of the double-sided capacitor container with the vapor that includes hydrogen fluoride, the etch initiator composition and alcohol comprises vapor phase etching a layer adjacent to the side wall of the double-sided capacitor container with the vapor that includes hydrogen fluoride, H_2O and an isopropyl alcohol.

16. A method of fabricating an integrated circuit, the method comprising:

housing the integrated circuit in a vapor etch chamber; and

vapor phase etching an insulator layer formed adjacent to a double-sided capacitor container in the integrated circuit, wherein the vapor phase etching of the oxide layer comprises inserting a vapor comprised of a hydrogen fluoride and isopropyl alcohol into the vapor etch chamber.

17. The method of claim 16, further comprising heating the hydrogen fluoride and the isopropyl alcohol prior to inserting the vapor into the vapor etch chamber.

18. The method of claim 16, wherein vapor phase etching the insulator layer formed adjacent to the double-sided capacitor container in the integrated circuit

comprises vapor phase etching a doped oxide layer formed adjacent to the double-sided capacitor container in the integrated circuit.

19. The method of claim 16, wherein vapor phase etching the insulator layer formed adjacent to the double-sided capacitor container in the integrated circuit comprises vapor phase etching a borophosphosilicate glass (BPSG) layer formed adjacent to the double-sided capacitor container in the integrated circuit.

20. The method of claim 16, wherein inserting the vapor comprised of hydrogen fluoride and isopropyl alcohol into the vapor etch chamber comprises inserting the vapor comprised of hydrogen fluoride, isopropyl alcohol and an etch initiator composition into the vapor etch chamber.

21. A method comprising:

placing a substrate that includes an array of memory into a chamber, the array of memory having at least one memory container with a side wall with an embedded capacitor; and

vapor phase etching of a layer of an insulator material formed adjacent to the side wall, wherein the vapor phase etching comprises:

mixing a hydrogen fluoride and an isopropyl alcohol to form a mixed vapor; and

inserting the mixed vapor into the chamber.

22. The method of claim 21, further comprising heating the hydrogen fluoride and the isopropyl alcohol prior to inserting the mixed vapor into the vapor etch chamber.

23. The method of claim 21, wherein mixing the hydrogen fluoride and the isopropyl alcohol to form the mixed vapor comprises mixing the hydrogen fluoride, the isopropyl alcohol and an etch initiator composition to form the mixed vapor.

24. The method of claim 21, wherein vapor phase etching of the layer of the insulator material formed adjacent to the side wall comprises vapor phase etching of a layer of oxide formed adjacent to the side wall.

25. The method of claim 21, wherein vapor phase etching of the layer of the insulator material formed adjacent to the side wall comprises vapor phase etching of a layer of silicon dioxide formed adjacent to the side wall.

26. A method for fabricating a semiconductor substrate, the method comprising:

placing the semiconductor substrate that includes a memory container into a vapor etching chamber, wherein a side wall of the memory container includes a double-sided capacitor; and

vapor phase etching of a layer of an insulator material formed adjacent to the side wall of the memory container, wherein the vapor phase etching comprises:

mixing an etch initiator composition, hydrogen fluoride and alcohol to form a mixed vapor;

heating the mixed vapor; and

inserting the mixed vapor into the vapor etching chamber.

27. The method of claim 26, wherein mixing the etch initiator composition, hydrogen fluoride and alcohol to form the mixed vapor comprises mixing the etch

initiator composition, hydrogen fluoride and isopropyl alcohol to form the mixed vapor.

28. The method of claim 26, wherein mixing the etch initiator composition, hydrogen fluoride and alcohol to form the mixed vapor comprises mixing the etch initiator composition, hydrogen fluoride and methanol to form the mixed vapor.

29. The method of claim 26, wherein vapor phase etching of the layer of the insulator material formed adjacent to the side wall of the memory container comprises vapor phase etching of a layer of silicon nitride formed adjacent to the side wall of the memory container.

30. The method of claim 26, wherein vapor phase etching of the layer of the insulator material formed adjacent to the side wall of the memory container comprises vapor phase etching of a layer of silicon oxynitride formed adjacent to the side wall of the memory container.

31. A method comprising:

placing a semiconductor substrate into a chamber; and

vapor phase etching of an insulator material formed adjacent to a double-sided container on a semiconductor substrate, wherein the vapor phase etching comprises:

forming a vapor that includes an H_2O vapor, an HF gas and a surface tension lowering agent; and

inserting the vapor into the chamber.

32. The method of claim 31, wherein forming the vapor that includes H_2O, hydrogen fluoride and the surface tension lowering agent comprises forming the vapor that includes H_2O, hydrogen fluoride and carboxylic.

33. The method of claim 31, wherein forming the vapor that includes H_2O, hydrogen fluoride and the surface tension lowering agent comprises forming the vapor that includes H_2O, hydrogen fluoride and alcohol.

34. The method of claim 31, wherein forming the vapor that includes H_2O, hydrogen fluoride and the surface tension lowering agent comprises forming the vapor that includes H_2O, hydrogen fluoride and isopropyl alcohol.

35. The method of claim 31, wherein forming the vapor that includes H_2O, hydrogen fluoride and the surface tension lowering agent comprises forming the vapor that includes H_2O, hydrogen fluoride and methanol.

36. The method of claim 31, wherein vapor phase etching of the insulator material formed adjacent to the double-sided container on the semiconductor substrate comprises vapor phase etching of a silicon dioxide material formed adjacent to the double-sided container on the semiconductor substrate.

37. The method of claim 31, wherein vapor phase etching of the insulator material formed adjacent to the double-sided container on the semiconductor substrate comprises vapor phase etching of a doped oxide material formed adjacent to the double-sided container on the semiconductor substrate.

38. A method for fabricating a memory array, the method comprising:

forming at least one memory container in a borophosphosilicate glass (BPSG) material on a substrate, wherein a side wall of the at least one memory container includes a double-sided capacitor; and

removing at least a part of the BPSG material based on a vapor wet etch operation with a vapor comprised of hydrogen fluoride and alcohol.

39. The method of claim 38, wherein removing the at least a part of the BPSG material based on the vapor wet etch operation with the vapor comprised of hydrogen fluoride and alcohol comprises removing the at least a part of the BPSG material based on the vapor wet etch operation with the vapor comprised of hydrogen fluoride and isopropyl alcohol.

40. The method of claim 38, wherein removing the at least a part of the BPSG material based on the vapor wet etch operation with the vapor comprised of hydrogen fluoride and alcohol comprises removing the at least a part of the BPSG material based on the vapor wet etch operation with the vapor comprised of hydrogen fluoride and methanol.

41. A method comprising:

forming at least one memory container in an oxide, wherein a side wall of the at least one memory container includes a double-sided capacitor; and

vapor wet etching of a layer of the oxide with a vapor comprised of hydrogen fluoride, an etch initiator composition and a surface tension lowering agent.

42. The method of claim 41, wherein forming the at least one memory container in the oxide comprises forming the at least one memory container in silicon oxide.

43. The method of claim 41, wherein vapor wet etching of a layer of the oxide with a vapor comprised of hydrogen fluoride, the etch initiator composition and a surface tension lowering agent comprises vapor wet etching of a layer of the oxide with a vapor comprised of hydrogen fluoride, the etch initiator composition and an alcohol.

44. The method of claim 41, wherein vapor wet etching of a layer of the oxide with a vapor comprised of hydrogen fluoride, the etch initiator composition and a surface tension lowering agent comprises vapor wet etching of a layer of the oxide with a vapor comprised of hydrogen fluoride, the etch initiator composition and an isopropyl alcohol.

45. The method of claim 41, wherein vapor wet etching of a layer of the oxide with a vapor comprised of hydrogen fluoride, the etch initiator composition and a surface tension lowering agent comprises vapor wet etching of a layer of the oxide with a vapor comprised of hydrogen fluoride, the etch initiator composition and methanol.

46. A vapor phase etching system comprising:

an etch initiator composition source;

a hydrogen fluoride source;

a surface tension lowering agent source;

a heater to receive an etch initiator composition from the etch initiator composition source, hydrogen fluoride from the hydrogen fluoride source and a surface tension lowering agent from the surface tension lowering agent source, the heater to heat the etch initiator composition, the hydrogen fluoride and the surface tension lowering agent to form a mixed vapor; and

a chamber to house a semiconductor substrate that includes at least one memory container, wherein a side wall of the at least one memory container includes a double-sided capacitor that is adjacent to an insulator layer, wherein the mixed vapor is to be inserted into the chamber.

47. The vapor phase etching system of claim 46, wherein the surface tension lowering agent comprises an alcohol.

48. The vapor phase etching system of claim 46, wherein the surface tension lowering agent comprises methanol.

49. The vapor phase etching system of claim 46, wherein the surface tension lowering agent comprises an isopropyl alcohol.

50. The vapor phase etching system of claim 46, wherein the insulator layer is an oxide layer.

51. The vapor phase etching system of claim 46, wherein the insulator layer is a silicon nitride layer.

52. The vapor phase etching system of claim 46, wherein the insulator layer is an silicon dioxide layer.

53. A system comprising:

a hydrogen fluoride source to output hydrogen fluoride;

an alcohol source to output alcohol;

a unit to receive the hydrogen fluoride and the alcohol and to generate a vapor comprised of the hydrogen fluoride and the alcohol; and

a chamber to hold a semiconductor substrate that includes a structure having a side wall that includes a double-sided capacitor adjacent to an oxide layer, wherein the vapor is to be input into the chamber.

54. The system of claim 53, wherein the alcohol includes methanol.

55. The system of claim 53, wherein the alcohol includes an isopropyl alcohol.

56. The system of claim 53, wherein the unit is to heat the vapor.

57. The system of claim 53, wherein the oxide layer comprises a silicon oxide layer.

58. The system of claim 53, wherein the oxide layer comprises a doped oxide layer.

59. A system comprising:

a processor to execute a number of instructions; and

a memory to store at least a part of the number of instructions, the memory having a number of memory cells, wherein the number of memory cells includes a double-sided capacitor fabricated in a side wall of a memory container, the number of memory cells fabricated by:

forming the memory container in an oxide; and

vapor wet etching of a layer of the oxide with a vapor comprised of a hydrogen fluoride, an etch initiator composition and a surface tension lowering agent.

60. The system of claim 59, wherein the surface tension lowering agent includes methanol.

61. The system of claim 59, wherein the surface tension lowering agent includes an isopropyl alcohol.

62. The system of claim 59, wherein the surface tension lowering agent includes carboxylic.

63. The system of claim 59, wherein the oxide comprises a silicon oxide.

64. An electronic system comprising:

a processor; and

a memory device comprising:

an array of memory cells having a number of double-sided capacitors formed in side walls of structures on a substrate, wherein the array of memory cells are formed by:

vapor phase etching of a layer of an insulator material formed adjacent to the side walls of the structures, wherein the vapor phase etching comprises:

mixing a hydrogen fluoride and an isopropyl alcohol to form a mixed vapor; and

inserting the mixed vapor into the chamber; and

an address decoder to decode access requests from the processor to access data in the array of memory cells.

65. The electronic system of claim 64, wherein the insulator material comprises a borophosphosilicate glass (BPSG) material.

66. The electronic system of claim 64, wherein the insulator material comprises silicon nitride.

67. The electronic system of claim 64, wherein the insulator material comprises a doped oxide.

68. The electronic system of claim 64, wherein the insulator material comprises silicon oxide.

69. An integrated circuit device comprising:

a first memory container having a side wall that includes a double-sided capacitor; and

a second memory container having a side wall that includes a double-sided capacitor, wherein the first memory container and the second memory container are

formed by vapor phase etching, with a vapor, an oxide layer between the side wall of the first memory container and the side wall of the second memory container, wherein the vapor includes a surface tension lowering agent.

70. The integrated circuit device of claim 69, wherein the surface tension lowering agent includes methanol.

71. The integrated circuit device of claim 69, wherein the surface tension lowering agent includes an isopropyl alcohol.

72. The integrated circuit device of claim 69, wherein the surface tension lowering agent includes carboxylic.

73. The integrated circuit device of claim 69, wherein the oxide layer comprises a silicon dioxide.

74. The integrated circuit device of claim 69, wherein the oxide layer comprises a doped oxide layer.

75. A memory device comprising:

an array of memory cells formed within a number of memory containers, a side wall of at least one of the number of memory containers having a double-sided capacitor, wherein the at least one of the number of memory containers is formed by vapor phase etching a layer adjacent to the side wall with a vapor that includes a surface tension lowering agent.

76. The memory device of claim 75, wherein the surface tension lowering agent includes methanol.

77. The memory device of claim 75, wherein the surface tension lowering agent includes an isopropyl alcohol.

78. The memory device of claim 75, wherein the surface tension lowering agent includes carboxylic.

79. The memory device of claim 75, wherein the surface tension lowering agent includes an acetic acid.

80. The memory device of claim 75, wherein the layer includes silicon dioxide.

81. The memory device of claim 75, wherein the layer includes a silicon nitride.

82. An integrated circuit comprising:

a substrate; and

a memory container formed on the substrate by:

forming the memory container in a borophosphosilicate glass (BPSG) material on the substrate, wherein a side wall of the memory container includes a double-sided capacitor; and

removing at least a part of the BPSG material based on a vapor wet etch operation with a vapor comprised of a hydrogen fluoride gas and an alcohol.

83. The integrated circuit of claim 82, wherein the alcohol includes methanol.

84. The integrated circuit of claim 82, wherein the alcohol includes an isopropyl alcohol.

85. An array of memory cells comprising:

a substrate; and

a structure having a side wall that includes a double-sided capacitor, wherein the structure is formed on the substrate by vapor phase etching a layer adjacent to the side wall with a vapor that includes methanol.

86. The array of memory cells of claim 85, wherein the layer includes an insulator material.

87. The array of memory cells of claim 85, wherein the layer includes a silicon dioxide.

88. The array of memory cells of claim 85, wherein the layer includes a silicon nitride.

89. A memory comprising:

a substrate; and

a number of memory containers having side walls that includes a double-sided capacitor, wherein the number of memory containers are formed on the substrate by etching an insulator layer adjacent to the side walls with a vapor that includes a hydrogen fluoride gas, an H_2O vapor and a surface tension lowering agent.

90. The memory of claim 89, wherein the insulator layer includes an oxide.

91. The memory of claim 89, wherein the insulator layer includes a doped oxide.

92. The memory of claim 89, wherein the surface tension lowering agent

93. The memory of claim 89, wherein the surface tension lowering agent includes an isopropyl alcohol.

94. The memory of claim 89, wherein the surface tension lowering agent includes carboxylic.

95. The memory of claim 89, wherein the surface tension lowering agent includes a trifluoroacetic acid.